

WAFER STAGE POSITION CALIBRATION METHOD AND SYSTEM

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor fabrication generally, and more specifically to methods for calibrating positional offset of a wafer stage.

BACKGROUND

[0002] A variety of metrology tools have been used to measure process performance on both monitor and product wafers. A general measurement may be taken at the wafer center. Typically, a measurement profile may be performed at a number of wafer sites to establish uniformity as a function of radial distribution or angle (theta). Stage repeatability and accuracy is a primary source of measurement drift. For example, a stage offset can impair the uniformity of film thickness in important layers, such as the gate oxide layer, reducing product yield. It has been determined that a stage offset of less than 2 mm can influence routine statistical process control (SPC) monitor status and unnecessarily impact tool availability. Traditional stage calibration sensitivity to stage drift is relatively weak.

[0003] Fourier transform infrared (FTIR) spectroscopy is a representative wafer metrology technique in that numerous measurement applications can be performed, such as oxide dopant concentration (Boron, Phosphorous, Fluorine), film thickness (epitaxial silicon, oxide, nitride, photoresist), and bare silicon impurity concentrations (interstitial oxygen, substitutional carbon). FTIR is sensitive to molecular absorption of light in the 2-40 μ m wavelength range. FTIR measurements can be performed using either transmitted or reflected mode. For example, transmission methods are typically used for calibrating position of a stage holding a bare silicon wafer. The wafer stage accommodates unobstructed illumination above and below the wafer using two vacuum "finger" supports located at a radius of 95 mm and theta 90 and 270 degrees.

[0004] The FTIR stage is calibrated interactively by visually aligning a HeNe laser image to center and edge scribe lines on a bare wafer. Another demonstrated calibration technique is based upon relative infrared signal strength for a wafer with pre-drilled aperture holes. Both methods are insensitive, and the time-intensive results show limited accuracy.

[0005] An improved wafer stage calibration method is desired.

SUMMARY OF THE INVENTION

[0006] A method of calibrating a positioning stage includes placing a substrate on the positioning stage. The substrate has a contrast film above a portion thereof, with at least one pattern at a predetermined location above the substrate, corresponding to a predetermined location on the positioning stage if the positioning stage has zero offset from a registration position. A beam is applied to a position where the pattern on the substrate would be located if the positioning stage has zero offset. At least one of the group consisting of reflected, transmitted and scattered portions of the beam is measured. Whether the positioning stage has a non-zero offset is detected based on the measured portion of the beam.

[0007] A monitor wafer comprises a semiconductor substrate; and a contrast film above the substrate. The contrast film includes a plurality of positive or negative patterns of geometrical objects distributed at a plurality of respectively different angles with respect to a reference location on the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1A is a diagram showing an exemplary system according to one embodiment of the invention using a negative photoresist.

[0009] FIG. 1B shows a frequency response of the signal detected by the sensor in FIG. 1A, when the calibration stage is offset in a first direction.

[0010] FIG. 1C shows a frequency response of the signal detected by the sensor in FIG. 1A, when the calibration stage has zero offset.

[0011] FIG. 1D shows a frequency response of the signal detected by the sensor in FIG. 1A, when the calibration stage is offset in a second direction opposite the first direction.

[0012] FIG. 2A is an isometric view of the monitor wafer of FIG. 1A.

[0013] FIGS. 2B-2D show frequency response of the signal detected by the sensor in FIG. 1A, when the calibration stage has an positive angle offset, a zero angle offset, and a negative angle offset, respectively.

[0014] FIG. 3A shows an exemplary system according to one embodiment of the invention using a positive photoresist.

[0015] FIGS. 3B-3D show frequency response of the signal detected by the sensor in FIG. 3A, when the calibration stage has an offset in a first direction, a zero angle offset, and an offset in a second direction opposite the first direction, respectively.

[0016] FIG. 4A is an isometric view of the monitor wafer of FIG. 3A.

5 [0017] FIGS. 4B-4D show frequency response of the signal detected by the sensor in FIG. 4A, when the calibration stage has an positive angle offset, a zero angle offset, and a negative angle offset, respectively.

[0018] FIG. 5 is a cross sectional view of a portion of a monitor wafer having two contrast layers.

10 [0019] FIG. 6 is a flow chart diagram of a method for calibrating and focusing a wafer stage.

[0020] FIG. 7 is a detailed flow diagram showing the steps of measuring and detecting translational and angular offsets.

DETAILED DESCRIPTION

15 [0021] This description of the exemplary embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical," "above," "below," "up," "down," "top" and "bottom" as well as derivative thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the
20 orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation.

[0022] The inventors have determined that, although the wafer stage may exhibit an offset and/or rotation from its nominal position, a standardized wafer can be centered on the
25 wafer stage accurately and consistently. Patterns can be formed on a standardized wafer with high dimensional accuracy. Thus, by optically or electronically monitoring the locations of the patterns on the monitor wafer that is centered on the stage, any positional offset of the wafer stage can be detected. By understanding the stage offset, the offset can be compensated for when measurements are taken from other bare wafers.

[0023] FIG. 1A is a diagram of a system for calibrating a positioning stage, such as wafer stage 100. The wafer stage 100 may be part of a metrology tool, for example.

[0024] A substrate, which may be a monitor wafer 110, is adapted to be placed on the wafer stage 100. The monitor wafer 110 has a substrate 120, which may be a semiconductor wafer (e.g., silicon, GaAs, or the like). The substrate 120 has a contrast film 130 on a portion thereof, with at least one pattern 135 at a predetermined location on the wafer. The contrast film may comprise at least one of the group consisting of photoresist, metal, oxide, and nitride. The monitor wafer may include an etch modified substrate. In the example of FIG. 1A, the contrast film 120 comprises a negative photoresist, and the pattern comprises one or more openings 135.

[0025] The predetermined location of the pattern 135 on the monitor wafer 110 corresponds to a predetermined location on the wafer stage, if the wafer stage has zero offset from a registration position. In other words, if the wafer stage has no offset, then the pattern 135 is accurately located at the predetermined location when the monitor wafer is centered on the wafer stage. If the wafer stage 100 has a translational or angular offset, then the pattern 135 is located at a position that deviates from the expected predetermined location.

[0026] A beam source 162 applies a beam 160 to a position where the pattern 135 on the wafer 110 would be located if the wafer stage 100 has zero offset. The beam source 162 may be a source of Microwave, Infrared, Visible, UV, or X ray radiation, or an electron beam source. In an exemplary embodiment, the beam source is an infrared source for FTIR spectroscopy.

[0027] A sensor measures at least one of the group consisting of reflected, transmitted and scattered portions of the beam. FIG. 1A shows a reflected portion 180 and a transmitted portion 190. A sensor 164 may be positioned to receive reflected light, and/or a sensor 165 may be positioned on the side of the substrate 120 opposite the beam source 162, to detect transmitted light (in which case the substrate 120 is formed of a transparent material, or a material having a high transmittance in the pertinent energy band of the incident beam 170). Although two sensors 164 and 165 are shown, the system may include a single sensor 164 above the substrate for only detecting reflected light 180, or the system may include a single sensor 165 on the bottom of the substrate 120 for measuring transmitted light 190 or scattered light.

[0028] One of ordinary skill in the art will understand that the substrate material and contrast film material should be selected so that there is a substantial difference in the optical properties of the two materials in the wavelength band corresponding to the beam source 162.

For example, to achieve the frequency responses shown in FIGS. 1B-1D using a negative resist for the contrast film, the reflectance of the contrast film 130 should be much greater than the reflectance of the substrate 120 in the relevant band.

[0029] The system includes means for detecting whether the wafer stage 100 has a non-zero offset based on the measured portion 180 of the beam 160. The detecting means is described in greater detail below. The detecting means includes computer program code for determining a position of the stage that minimizes or maximizes the signal 180.

[0030] FIGS. 1B-1D show three exemplary FTIR frequency responses of reflected light that may be observed by the sensor 164, depending on the magnitude of the stage offset, where the stage offset may have a negative value, a zero value, or a positive value. In FIGS. 1B-1D, the frequency response of transmitted light is ignored, but in other examples, the transmitted light may be considered. For a contrast film 120 comprising a negative photoresist, in which the pattern comprises one or more openings 135, the measured portion 180 of the beam 160 has a first frequency distribution shown in FIG. 1C if the wafer stage has a zero offset. The frequency response is very flat, and may be approximately zero. FIG. 1B shows a second frequency response of the signal 180 observed if the wafer stage has a non-zero offset, or stage axis error 150. In the example, the same second frequency response is observed when the offset 150 is a negative value as when the offset is a positive value with the same magnitude.

[0031] Given a stage offset 150 of magnitude D (yielding a response as shown in FIG. 1B or 1D), the signal 180 can be minimized (as shown in FIG. 1C) by moving the wafer stage by a distance of -D. Once the total stage displacement needed to reach the frequency response of FIG. 1C is measured, the wafer stage offset 150 can be readily determined as (-1) times the displacement through which the stage is moved to minimize the signal 180.

[0032] Although FIG. 1A shows the stage offset (stage axis error) in the Y dimension, the same method is used for the orthogonal direction X (into and out of the page) in the plane of the wafer 110. The only difference is that the stage is moved in the X direction to minimize the frequency response of signal 180. Note that, because there may be positional errors in both the X and Y directions, minimizing the frequency response of signal 180 by compensating for the stage axis error in one direction can still leave a significant non-zero signal 180 due to stage offset (axis error) in the orthogonal direction. Nevertheless, minimizing the signal 180 with

respect to movement of the stage along a single direction at a time (X or Y) locates the optimum position along that direction.

[0033] A variety of techniques may be used to find the minimum frequency response position. The stage can be controlled manually, using trial and error. Automated control methods may also be used. For example, an initial interval extending on both sides of the zero offset stage position can be selected (large enough to have a high degree of probability of including the stage position that produces the minimum response). An initial small displacement increment may be selected, and the stage can be moved through the initial interval using that initial increment. The frequency response is measured again at each incremental position. When a local minimum is observed, the interval is reduced so that the beginning and end of the interval are the two nearest positions on either side of the local minimum. The increment can be reduced (e.g., by one half), and the stage can be moved between the two positions on either side of the local minimum. This procedure can be repeated, reducing the interval through which the stage is traversed between the points on either side of the local minimum at each iteration. When the interval is reduced to any desired value, then the location of the absolute minimum has been determined with a maximum error equal to the size of the interval during the last iteration. A variety of other numerical techniques may be used to automatically search for the wafer stage position at which the frequency response is minimized.

[0034] Although the above example relates to stage position offsets, a similar result is observed when there is a stage focus error 192. By moving the stage in the direction orthogonal to the plane of the wafer 120 (e.g., up or down), the frequency response of signal 180 varies, with a minimum occurring when the stage is at the optimum stage focus position in the Z direction. The stage focus error is then determined as being (-1) times the Z distance through which the stage is moved to minimize the signal 180.

[0035] FIG. 2A is an isometric view of the wafer 110. Preferably, the wafer includes a plurality of patterns of geometric objects 135. In FIG. 2A, the geometric objects are rectangles, but any shape may be used. Rectangles are advantageous because they may simplify computations relative to other geometric shapes. Further, if scattered light is to be measured, then the patterns may be diffraction gratings (not shown), for example, comprising groups of parallel lines.

[0036] In preferred embodiments, the contrast film 130 includes a plurality of positive or negative patterns comprising geometrical objects distributed at a plurality of respectively different angles with respect to a reference location (e.g., the notch 122) on the substrate. In the example of FIG. 2A, the patterns include four rectangles 135 spaced 90 degrees apart and located proximate to a circumference of the monitor wafer. In another embodiment, the wafer has eight rectangles spaced 45 degrees apart. A central rectangle is also provided. Wafer 110 also has a notch 122 which establishes a zero-reference angle along the circumference of the wafer. In alternative embodiments, several patterns 135 may be placed near the center, with zero or fewer patterns near the circumference of the wafer.

[0037] In preferred embodiments, the wafer includes at least a second pattern 135 disposed at a different angular position on the wafer from the first pattern, to enable wafer stage angular offset 194. The system further comprises means for determining a translation vector separating the first and second patterns, and means for detecting an angular offset 194 of the wafer stage, based on the translation vector.

[0038] The translation determining means identifies a stage position corresponding to one of the patterns 135, as described above. The stage is then moved by an "expected translation vector" (corresponding to the expected zero-angular-offset position of the second pattern), so that the beam 170 is focused on the approximate location of the second pattern (e.g., a pattern that is 180 degrees apart from the first pattern). For example, the stage may be moved by the distance that would be correct for focusing the beam 170 on the second pattern if there is no stage angular offset. If there is an angular offset 194, then an expected translation vector corresponding to the expected (zero angular offset) position of the second pattern results in a substantial frequency response signal 180. The actual location of the second pattern is determined iteratively by moving the stage until the signal 180 is minimized, in the manner described above with respect to FIGS. 1A-1D. The frequency response for positive, zero and negative stage angle offsets would be similar to those shown in FIGS. 2B, 2C and 2D, respectively. By subtracting the location of the first pattern from the actual location of the second pattern, the "actual translation vector" between the two is identified. The angle between the "actual translation vector" and the "expected translation vector" corresponds to the angular offset of the wafer stage.

[0039] FIGS. 3A-3D and 4A-4D show how the methods of FIGS. 1A-1D and 2A-2D, respectively, would be performed if the monitor wafer 310 contains positive patterns 330 of

geometric objects. The exemplary wafer 310 includes a substrate 320 with a positive pattern of a contrast film, which may be an organic photoresist. Alternative contrast film materials may include metal, oxide, or nitride, or an etch modified substrate may be used.

[0040] The beam source 362 provides a beam 360 including incident radiation 370. A sensor 364 collects a reflected portion 380 of the beam. In other embodiments, the sensor 364 is located below the wafer 310 and detects a transmitted portion 390 of the beam, or a diffracted beam (not shown). The frequency response of the signal 380 is analyzed.

[0041] As shown in FIGS. 3B-3D, in the case of a positive pattern on a transparent substrate, the frequency response is maximized when the beam 370 is directed on the pattern. If the beam is off the pattern, then the frequency response is much lower, and may be approximately zero. Thus, in order to detect an offset, the wafer stage is positioned with the expected position of one of the patterns 330 in the field of view of the incident beam 370. If the frequency response is small, the wafer stage is reiteratively moved until the signal is maximized, corresponding to the stage at its optimal position. The wafer stage offset 350 is then determined as the distance between the expected position for maximum signal 380 and the actual position for maximum signal. Similarly, the stage focus offset error 392 can be determined by raising and lowering the wafer stage 100 until the detected signal 380 is maximized, to determine the location for the optimum focus, and the offset between the optimum focus and the expected height of the stage for optimum focus.

[0042] FIGS. 4A-4D show the exemplary wafer having a plurality of positive patterns 330 on the substrate 320. The procedure for determining the stage angular offset is similar to that described above with reference to FIGS. 2A-2D, except that the actual locations of the patterns 330 are found by maximizing the frequency response of the signal 380, as shown in FIGS. 4C. An expected translation vector between a first one of the patterns 330 and a second one of the patterns is calculated, and an actual translation vector is determined based on the measured signals 380 (and/or 390). The angle between these two vectors corresponds to the stage angular offset 394.

[0043] FIG. 5 is a cross sectional view of an "etch-modified" wafer 520 having a multi-layer pattern thereon. A pattern 530 similar to the patterns 330 described above with reference to FIGS. 3A-4D is formed above the substrate 520. At least one additional layer 532 is formed above the first pattern layer 530. The pattern 532 is preferably smaller than the pattern 530, to

form a step at each edge, so that an incident beam can be reflected off of both edges. The detecting means determines whether the wafer stage has an offset based on the measured portion of the beam reflected, transmitted or scattered portions from the first film and the measured portion of the beam reflected, transmitted or scattered portions from the second film.

5 [0044] In some scenarios, the frequency responses of the two layers 530 and 532 may differ from each other, so that a high signal value is detected in a first one of the layers at a frequency for which the other of the layers has a low signal value. By combining the results of both signals, it becomes easier to distinguish the optimum location of the wafer stage.

10 [0045] In some embodiments, the plurality of geometrical objects includes a plurality of first rectangular contrast film portions 530, and the monitor wafer further includes a plurality of second rectangular contrast film portions 532 on one or more of the first rectangular contrast film portions. In other embodiments, either the first portions 530 or the second portions 532 may have non-rectangular shapes. In some embodiments, the first and second layers 530 and 532 formed for each of the patterns of geometric objects.

15 [0046] In one example, the substrate 520 is silicon, the first film 530 is a silicon oxide, and the second film 532 is a photoresist.

[0047] Although FIG. 5 shows an example in which a positive pattern is deposited on the substrate, in other embodiments (not shown), two contrast film layers are formed on the substrate; both contrast layers are etched to form openings all the way to the substrate, with the
20 openings in the top contrast layer larger than the openings in the bottom contrast layer. This provide an alternative way to achieve a stepped configuration of two contrast layer materials.

[0048] FIG. 6 is a flow chart showing an example of one process for calibrating wafer stage offsets 150, focus errors 192 and angular offsets 194.

[0049] At step 602, (for a negative film pattern) a contrast film is deposited on a bare
25 wafer. The photo-resist film is deposited and evaporated onto the bare wafer or a wafer with a deposited film of interest.

[0050] At step 604, in some embodiments, the contrast film is etched to form patterns comprising geometric objects in the monitor wafer. If a negative photoresist is used, the patterns are typically etched, and the remainder of the contrast film is masked. If a positive photoresist is
30 used, the patterns are typically masked, and the remainder of the contrast film is etched.

[0051] Generally, using the clear out window on any reticle, specified target areas and patterns are exposed and developed. For simplicity, a 6 mm square void window may be used; films composed of materials other than photoresist (metals, oxides/nitrides, etch-modified substrates, etc.) using a variety of target sizes and patterns can be developed for metrology tool-specific requirements.

[0052] An exemplary calibration wafer designed for infrared calibration is produced using two routine photo process steps:

[0053] A typical photo process includes the following eight steps:

[0054] • Expose wafer to Hexamethyldisilazane (HMDS) to make the surface hydrophilic.

[0055] • Coat wafer with sufficient photo-resist

[0056] • Pre-Exposure

[0057] • Expose the wafer to a desired pattern (an exemplary method uses clear out windows)

[0058] • Bake after exposure

[0059] • Develop and Rinse

[0060] • Post Develop Bake

[0061] With this method wafer positional accuracy of approximately $3\mu\text{m}$ is achieved and the pattern can be controlled to micron size.

[0062] At step 605, the monitor wafer is placed on the wafer stage, with at least one pattern at a predetermined location on the wafer, corresponding to (lying directly above) a predetermined location on the wafer stage if the wafer stage has zero offset from a registration position.

[0063] At step 606, a beam is applied to a position where the pattern on the wafer would be located if the wafer stage has zero offset. At least one of the group consisting of reflected, transmitted and scattered portions of the beam is measured, and detected portions of the beam are analyzed.

[0064] At step 608, the system detects whether the wafer stage has one or more non-zero offsets based on the measured portion of the beam. The X and Y offsets are determined, based on the distance the stage must be moved to find the optimum position (minimum signal for a negative contrast material pattern, maximum signal for a positive contrast material pattern.

[0065] At step 610, a location of at least a second pattern is determined, from which the translation vector separating the first and second pattern is determined.

[0066] At step 612, the translation vector is compared to the expected translation vector.

[0067] At step 614, an angular offset is detected, based on the comparison of step 612.

5 [0068] At step 616, a stage focus error, if any, is detected based on the Z offset (i.e., on the distance the stage is raised or lowered to achieve the optimum signal return 192.

[0069] Although an exemplary sequence of operations is shown in FIG. 6, other sequences may be used. For example, the beam focus can be calibrated before the X and Y offsets are determined, or between determining the X and Y offsets and the angular offset.

10 [0070] FIG. 7 is a more detailed flow diagram of a calibration process. Some of the steps in FIG. 7 may be performed by the detecting means (including steps 708, 714, 716, 718, 722, 724).

[0071] At step 702 the monitor wafer is placed on the metrology tool wafer stage. This may be performed by a robot end effector, or other robotic arm or pick and place device (not
15 shown).

[0072] At step 704, a loop including steps 706-724 is performed for each of a plurality of calibration patterns (or markings). If the wafer has several calibration patterns, the loop may be performed for all of the patterns or for a subset of the patterns. To allow angle offset detection, the loop is repeated for at least two of the patterns.

20 [0073] At step 706, a loop including steps 708-722 is repeated for X, Y and Z directions.

[0074] At step 708, the total distance moved is reset to zero.

[0075] At 710, the beam source applies the beam to the zero-offset position where the pattern is expected (i.e., where the pattern would be if there is no stage position error.

[0076] At step 712, the sensor detects the reflected, transmitted and/or scattered
25 portion(s) of the beam.

[0077] At step 714, the detecting means analyzes the frequency response of the measured portion of the beam.

[0078] At step 716, the detecting means determines whether the stage has a non-zero stage offset based on the measurement. If a negative resist is used, then a high frequency
30 response indicates a non-zero offset. If a positive resist is used, then a low, flat frequency response indicates a non-zero offset.

[0079] At step 718, if an offset has been detected, step 720 is executed. If no offset has been detected, then step 722 is executed.

[0080] At step 720, the wafer stage is moved incrementally, and the detecting means loops back to step 710. Steps 710-718 are repeated, until no offset is detected at step 716.

5 [0081] At step 722, the magnitude of the offset in the X direction is determined by the total distance the wafer stage is moved in the X direction to achieve the optimum frequency response. The magnitude of the offset in the Y direction is determined by the total distance the wafer stage is moved in the Y direction to achieve the optimum frequency response of the movement.

10 [0082] At step 724, the direction of the offset (within the plane of the wafer) is determined based on the X and Y offsets.

[0083] The calibration wafers described above can be prepared without wafer damage and/or operator interaction. Additionally, the calibration technique can be performed under standard operating conditions with no recovery period between calibration and operation.

15 Calibration location accuracy of nanometer scale is achievable and can be routinely performed at multiple wafer locations.

[0084] The methods described above can provide faster wafer stage calibration. Improved, highly accurate calibration criteria may be used. Optionally, a complex calibration pattern, spot size, wafer property gradient may be used. Standard instrument operating
20 conditions can be retained.

[0085] The system can provide early tool drift warning and notification. The system can also provide component specific stage drift determination including x and y stage motion controllers (belts, motors, etc.), wafer flat (notch) finder calibration, and hardware failures. For example, if the center of the stage has zero positional offset, but the patterns on the perimeter are
25 offset (by an angle), then this indicates that there may be a problem with the flat finder. A pure X-Y translation is an indication of a drive train problem, such as a belt or motor problem. Typically, if the drive train problem is observed sporadically, it is more likely a belt problem. If the problem is observed consistently, it is more likely a motor problem. Stage motion restriction determination is possible, i.e. cable tension, mechanical blockage. Optical degradation can be
30 detected, such as scattering, defocusing, and the like, related to optical component condition and

alignment, including source, detector, interferometer/ monochromometer/ modulator, relay optics, instrument environment, optical windows.

[0086] Although the examples described above include a special purpose monitor wafer, with the contrast film formed on the bare semiconductor, any wafer may be used for the stage offset calibration method by placing the desired patterns on the wafer. Thus, the patterns may be on a layer above the surface of the substrate, with one or more intervening layers therebetween. More generally, any solid substrate including a top surface having patterns with predetermined locations may be used. The substrate is not limited to silicon or any specific semiconductor material, and is not limited to a disc or circular shape.

[0087] The present invention may include computer-implemented processes and apparatus for practicing those processes. The present invention may also be embodied in the form of computer program code embodied in tangible media, such as floppy diskettes, read only memories (ROMs), CD-ROMs, hard drives, ZIPTM disks, memory sticks, or any other computer-readable storage medium, wherein, when the computer program code is loaded into and executed by a computer, the computer becomes an apparatus for practicing the invention. The present invention may also be embodied in the form of computer program code, for example, whether stored in a storage medium, loaded into and/or executed by a computer, or transmitted over some transmission medium, such as over the electrical wiring or cabling, through fiber optics, or via electromagnetic radiation, wherein, when the computer program code is loaded into and executed by a computer, the computer becomes an apparatus for practicing the invention. When implemented on a general-purpose processor, the computer program code segments configure the processor to create specific logic circuits.

[0088] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.